

REMARKS

Claims 1-23 are pending in the case. The Examiner rejected claims 1, 2, 8-11, and 17-18 under 35 U.S.C. §103(a) as being unpatentable in view of U.S. Patent No. 6,549,988 to Gertner (hereinafter "Gertner") in view of U.S. Patent No. 6,226,111 to Chang et. al. (hereinafter "Chang"). The Examiner rejected claims 3, 6, 12, and 15 under 35 U.S.C. §103(a) as being unpatentable in view of Gertner, Chang, and U.S. Patent No. 6,101,166 to Baldwin (hereinafter "Baldwin"). The Examiner rejected claims 4, 5, 13, and 14 under 35 U.S.C. §103(a) in view of Gertner, Chang, Baldwin, and U.S. Patent No. 6,725,293 to Nakayama et. al. (hereinafter "Nakayama"). The Examiner rejected claims 7 and 16 under 35 U.S.C. §103(a) as being unpatentable in view of Gertner, Chang, and U.S. Patent No. 5,966,487 to Gilliland et al. (hereinafter "Gilliland").

The Examiner rejected claims 19-21 under 35 U.S.C. §102(e) in view of Nakayama. The Examiner rejected claim 22 under 35 U.S.C. §103(a) in view of Nakayama. The Examiner rejected claim 23 under 35 U.S.C. §103(a) in view of Nakayama and Gilliland.

Applicant respectfully asserts that based on the following remarks Claims 1-23 are patentable over the prior art of record and the rejections set forth above. Applicant respectfully requests the prompt allowance of Claims 1-23.

REJECTION OF CLAIMS 1, 2, 8-11, AND 17-18 UNDER 35 U.S.C. §103(a)

The Examiner rejected claims 1, 2, 8-11, and 17-18 under 35 USC §103(a) in view of Gertner and Chang. Applicant respectfully traverses this rejection.

Prima Facie Obviousness.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness, the combination of the prior art references must teach or suggest all the claim limitations. *See id.* Furthermore, even if all the claim limitations are taught or suggested, there must be some suggestion or motivation to combine reference teachings. *See* MPEP §2142. Furthermore, "The teaching or suggestion to make the claimed combination ... must be found in the prior art, not in applicant's disclosure."

MPEP §2143, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Applicant respectfully asserts that a *prima facie* case of obviousness has not been made because all the elements recited in the claims are NOT taught or suggested by the prior art and there is no teaching or suggestion in the art to combine the references to produce the claimed invention. In particular, Applicant respectfully asserts that Gertner and Chang fail to teach or suggest all the claim limitations of the independent claims 1, 9, 18, and 19.

Claim 1 is representative of the subject matter in the other independent claims and recites in pertinent part "...a loop healing switch coupled to the first loop and the second loop, wherein upon detection of a failure the loop healing switch couples the first loop and the second loop." (emphasis added). Applicant submits that while Gertner and Chang discuss dual ring network topologies and self-healing through path protection, respectively, these references fail to teach active coupling of a first loop to a second loop in response to a failure (upon detection). Instead, these references teach redundant paths each carrying duplicate signals such that failure of a link or node is accommodated in a passive manner. Consequently, the healing solution proposed in Chang uses more equipment (dual paths) but does not gain an increase in available bandwidth.

Gertner.

Gertner teaches use of a Fibre Channel Arbitrated Loop (FCAL) and a fibre channel switch to interconnect a plurality of hosts 112 and storage devices 161, 171. See Gertner Col. 5, lines 25-37. Gertner also mentions that the fibre channel may comprise two FCAL loops connected via a switch. The Examiner correctly notes that Gertner fails to teach a loop healing switch upon detection of a failure.

Chang.

Chang teaches a cross-connect for a multi-ring multi-channel network. See Chang Abstract. Chang points out that the inter-connected rings are self-healing due to a redundant count-rotating ring. See *Id.* Chang employs different configurations of NxN switches to provide a protection path between rings connecting the nodes.

The Examiner suggests that Chang teaches "...a loop healing switch coupled to the first loop and the second loop, wherein upon detection of a failure the loop healing switch couples the first loop and the second loop" as recited in Claim 1. While Chang does teach automatic healing of a dual ring topology, Chang fails to teach the loop healing switch recited in Claim 1 that actively couples the first loop and the second loop in response to a failure.

Instead, Chang teaches a redundant system of rings with signals passing unidirectionally in opposite directions. *See* Chang Col. 11, lines 1-3, Fig. 7. Chang describes a network of two rings with each ring having a redundant protection ring. *See* Chang Col. 11, lines 6-8. Chang points out that the working and protection rings need not be interconnected because the path protection topology employs has the working and protection rings carrying the same information. *See* Chang Col. 11, lines 21-23. This means that for Chang to implement a dual ring 52<sub>1</sub>, 52<sub>2</sub> topology Chang must have twice as much network transport medium (fibre).

Next, Chang explains how the self-healing aspect operates. Chang explains that the 3x3 switches serve as cross-connects for the respective working and protection rings. *See* Chang Col. 11, lines 27-29. The cross-connects enable nodes coupled to one ring 52<sub>1</sub> to interface with nodes of the other ring 52<sub>2</sub>. Chang includes a cross-connect controller that ensures that both 3x3 switches are in the same switching state. *See* Chang Col. 11, lines 30-33. This means paths are preconfigured and predefined in Chang. The switches 60,62 are preconfigured so that "if a failure occurs in either of the working fibers 54<sub>1</sub>, 54<sub>2</sub>, the protection fibers 56<sub>1</sub>, 56<sub>2</sub>, are already properly interconnected...so that the cross-connect controller 72 does not need to reconfigure the 3x3 switches 60, 62 in response to a failure." *See* Chang Col. 11, lines 34-39.

Therefore, Applicant asserts that Chang teaches a passive form of self-healing in which switches are preconfigured and synchronized such that failures can be circumvented. Chang include no logic to actively respond to a failure to perform the self-healing. If the switches connecting the working and protection fibers in Chang are not preconfigured and set communication in the Chang network would be severely disrupted. Chang does teach active configuration of the switches using the cross-connect controller 72 but this is "only in response to long-term changes in the traffic pattern" not automatically detected failures. *See* Chang Col. 11, lines 40-45.

In stark contrast, as recited in Claim 1, "upon detection of a failure the loop healing switch couples the first loop and the second loop." The loop healing switch include appropriate logic to detect a failure in one of the loops and respond by coupling the two loops so that interconnectivity is not lost. The logic that performs this operation is described in relation to Figure 2 and includes the cooperation of the Port Bypass Circuits (PBC) 220, 250 and the Host Port Good (HPG) control signals provided by the Loop Resiliency Circuits (LRC) 140-143 (Figure 1). Active switching into a failure mode is described in the specification on page 8 line 23 through page 9 line 9. The present invention includes logic to actively interconnect the two rings in response to the failure but keeps the rings separate to provide higher bandwidth when no failure has been detected.

Chang, in contrast, does not interconnect the working fiber and protection fiber. (See Chang Col. 11, lines 21-24.) However, Chang does interconnect the two loops, including synchronizing the switching states and traffic, so that should a failure occur the nodes remain interconnected. This interconnection of the loops limits the bandwidth available to the nodes.

Therefore, Applicant asserts that Chang fails to teach a main element of the independent Claims 1, 9, 18, and 19. These claims specifically set forth that the present invention actively couples the first and second loops once a failure is detected. The loops are not pre-connected and configured as is taught in Chang. Because the combination of the prior art references must teach or suggest all the claim limitations, Applicant asserts that a *prima facie* case of obviousness has not been made.

Furthermore, because Chang fails to teach a main element of the independent claims, Applicant fails to see why one of skill in the art would combine Gertner and Chang. Such a combination would still come up short of the present invention. Finally, Applicant finds no motivation, teaching, or suggestion in Gertner or Chang to make such a combination.

For the reasons stated above, Applicant respectfully submits that Claims 1, 9, 18, and 19 and dependents thereof including claim 2, 8-11, and 17-18 are in condition for allowance and nonobvious in view of the prior art of record.

**REJECTION OF CLAIMS 3, 6, 12, AND 15 UNDER 35 U.S.C. §103(a)**

The Examiner rejected claims 3, 6, 12, and 15 under 35 USC §103(a) in view of Gertner, Chang, and Baldwin. Applicant respectfully traverses this rejection.

Claims 3, 6, 12, and 15 depend respectively from independent Claims 1 and 8 and include all the limitations thereof. Applicant has explained above where Gertner and Chang fail to teach all the elements of Claims 1 and 8. Baldwin fails to provide the teachings missing in Gertner and Chang to support a *prima facie* case of obviousness with respect to Claims 3, 6, 12, and 15. Therefore, Applicant submits that Claims 3, 6, 12, and 15 are nonobvious in view of Gertner, Chang, and Baldwin.

**Baldwin.**

Baldwin seems to teach a port bypass circuit the bypasses a port in response to a port failure. *See* Baldwin Abstract. Baldwin does require that the failed port send failure initialization data. *Id.* Baldwin fails to include any teachings regarding a loop healing switch as recited in the independent Claims 1 and 8.

In addition, Claims 3, 6, 12, and 15 teach loop resiliency circuits (LRCs) that include a Signal Detection Unit (SDU). The SDU monitors the condition of incoming fibre channel signals and signals a failure in response to these signals failing to meet minimum requirements. See Specification page 9, lines 12-16. Therefore, the present invention does not require failure initialization data from a port.

Therefore, Applicant submits that Claims 3, 6, 12, and 15 are nonobvious in view of Gertner, Chang, and Baldwin.

**REJECTION OF CLAIMS 4, 5, 13, AND 14 UNDER 35 U.S.C. §103(a)**

The Examiner rejected claims 4, 5, 13, and 14 under 35 USC §103(a) in view of Gertner, Chang, Baldwin, and Nakayama. Applicant respectfully traverses this rejection.

Claims 4, 5, 13, and 14 depend respectively from independent Claims 1 and 8 and include all the limitations thereof. Applicant has explained above where Gertner, Chang, and Baldwin fail to teach all the elements of Claims 1 and 8. Nakayama fails to provide the teachings missing in Gertner, Chang, and Baldwin to support a *prima facie* case of obviousness with respect to

Claims 4, 5, 13, and 14. Therefore, Applicant submits that Claims 4, 5, 13, and 14 are nonobvious in view of Gertner, Chang, Baldwin, and Nakayama.

Nakayama.

Nakayama teaches a storage controller that utilizes fibre channels and interconnects a plurality of host computers having different interfaces. *See Nakayama Abstract.* The storage controller of Nakayama includes a plurality of host interface controllers (HIFC) and redundant control processors that process I/O requests from hosts. *See Nakayama Col. 3, lines 5-19.* The HIFCs and control processors are connected by a loop described in relation to Figure 2. *See Nakayama Col. 4, lines 21-52.* Nakayama further teaches that the control processors monitor the operation status of each other and take over processing for failed control processors. *See Nakayama Col. 6, lines 22-39.* The control processors also monitor workload for each other and work to balance the workload. *See Nakayama Col. 6, lines 43-45.*

Claims 4, and 13 recite port bypass circuits (PBCs) and Signal Detection Units (SDUs) within loop resiliency circuits (LRCs). The SDU detects a failure of a controller and then disconnects the controller from the loop. Applicant acknowledges that Nakayama teaches control processors that monitor and take over for each other. However, Applicant fails to see where Nakayama teaches that one control processor disconnects a failed control processor from the loop as recited in Claims 4 and 13. Claims 5, and 14 recite a logic module that "check[s] for the presence of a loop port enable signal." If a fault signal is detected on the loop port enable signal, the logic module signals the loop healing switch to couple the first and second loops. Applicant also fails to see where Nakayama teaches a logic module that signals a loop healing switch to couple a first and second loop.

Furthermore, Nakayama fails to teach or disclose a loop healing switch that is also missing from Gertner, Chang, and Baldwin. Therefore, Applicant submits that Claims 4, 5, 13, and 14 are nonobvious in view of Gertner, Chang, Baldwin, and Nakayama.

**REJECTION OF CLAIMS 7 AND 16 UNDER 35 U.S.C. §103(a)**

The Examiner rejected claims 7 and 16 under 35 USC §103(a) in view of Gertner, Chang, and Gilliland. Applicant respectfully traverses this rejection.

Claims 7 and 16 depend respectively from independent Claims 1 and 8 and include all the limitations thereof. Applicant has explained above where Gertner and Chang fail to teach all the elements of Claims 1 and 8. Gilliland fails to provide the teachings missing in Gertner and Chang to support a *prima facie* case of obviousness with respect to Claims 7 and 16. Therefore, Applicant submits that Claims 7 and 16 are nonobvious in view of Gertner, Chang, and Gilliland.

**Gilliland.**

Gilliland teaches a media interface adapter module for converting between a copper transfer medium and another transfer medium. *See* Gilliland Abstract. Gilliland includes no teachings or suggestions of a loop healing switch as recited in the independent claims upon which Claims 7 and 16 depend. Therefore, Applicant submits that Claims 7 and 16 are nonobvious in view of Gertner, Chang, and Gilliland.

**REJECTION OF CLAIMS 19-21 UNDER 35 U.S.C. §102(e)**

The Examiner rejected claims 19-21 under 35 U.S.C. §102(e) in view of Nakayama. Applicant respectfully traverses this rejection.

The Federal Circuit has made clear that “[a]nticipation under 35 U.S.C. §102 requires the disclosure in a single piece of prior art of each and every limitation of a claimed invention.” *Apple Computer, Inc. v. Articulate Systems, Inc.*, 234 F.3d 14, 20, 57 U.S.P.Q.2d 1057, 1061 (Fed. Cir. 2000). Furthermore, the “identical invention must be shown in as complete detail [in the prior art] as is contained in the . . . claim” of the present invention. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Applicants respectfully assert that Nakayama fails to teach or disclose each element of the claimed invention as required under 35 U.S.C. §102(e).

Claim 19 recites:

“...evaluating signals from a first controller coupled to a first loop to check for a failure; evaluating signals from a second controller coupled to a second loop to check for a

failure; and upon detection of a failure affecting one of the first controller and the second controller, coupling the first loop to the second loop so as to provide a plurality of host servers access to a surviving controller."

The Examiner suggests that the elements of this claim are taught in Nakayama at Col. 6, lines 13-58. Applicant respectfully disagrees. The Examiner may be able to read the first two elements broadly as being taught by Nakayama. However, a close analysis of Nakayama will show that there is no "coupling of the first loop to the second loop so as to provide a plurality of host servers access to a surviving controller." In fact, to make such a coupling in Nakayama is irrational and unnecessary.

A review of Nakayama including Col. 6, lines 13-58 and Figure 1 indicates that Host Interface Controllers connect to control processors via a Fibre channel loop 133. *See* Nakayama Col. 3, lines 5-10. The bus 118 connects the control processors 114-117 to the memory 122, 112, service processor 131, and a pair of control processors 119 and 120. The control processors 119 and 120 connect via fibre channel loops 141 to drive interface controllers 123, 124 which are connected to drives 127-130 by loops 125 and 126. *See* Nakayama Col. 3, lines 13-19.

Thus, there are five different loops discussed in Nakayama: loop 133, loop 141 (second loop 141 does not have a reference numeral), and loops 125 and 126. Interpreting Nakayama with respect to these loops and Col. 6, lines 13-58 in its most favorable light with respect to the Examiner's position still fails to disclose "...each and every limitation of a claimed invention."

Although, Nakayama uses the same name for the control processors 114-117 and control processors 119 and 120. The different reference numerals indicate that Nakayama considers the two sets of control processors 114-117 and control processors 119 and 120 very differently. Specifically, when Nakayama intends to discuss common features, the two kinds of control processors are grouped together as in Col. 3, lines 49-51. When Nakayama intends to discuss different features, the two kinds of control processors are separately numbered and discussed as in Col. 4, lines 13-20 where control processors 119 and 120 serve as gatekeepers for the drives 127-130.

In Col. 6, lines 13-21 control processors 119 and 120 are discussed. Nakayama teaches that either control processor 119 or 120 can process the I/O requests. Each control processor 119

and 120 serves as a redundant back up for the other. There is no teaching in Nakayama of an evaluation of control processor 119 or 120 for a failure. Therefore, the Examiner relies on Col. 6, lines 22-57 where control processors 114-117 are specifically referenced as having the functionality to monitor each other. However, control processors 114-117 are not coupled to a first loop and a second loop as required in Claim 19. Control processors 114-117 are coupled to a single loop, loop 133. Under a very broad and unreasonable interpretation of the term "coupled," the control processors 114-117 may be said to be coupled to the loops 125 and 126. Even so, Nakayama still fails to teach the last element of Claim 19.

If one control processor 114-117 detects failure of another control processor 114-117, Nakayama teaches that the control processor 114-117 takes over handling I/O requests for the failed control processor 114-117. However, in doing so the first loop and second loop are to be coupled "...so as to provide a plurality of host servers access to a surviving controller." If the first loop and second loop are loops 125 and 126, as proposed by the Examiner, Applicant fails to see how coupling loops 125 and 126 provides the hosts 100-102 access to the surviving controller 114-117. The hosts 100-102 always had access to the surviving controller 114-117 regardless of what happens with loops 125 and 126. Applicant finds the interpretation proposed by the Examiner irrational given the configuration and teachings of Nakayama. There is no reason for coupling loops 125 and 126 because the hosts 100-102 do not gain any interconnectivity advantage. Applicant respectfully submits that this inconsistency in the Examiner's interpretation indicates that Nakayama fails to teach each and every element of Claim 19.

Claims 20 and 21 depend from Claim 19 and are therefore allowable for at least the same reasons.

**REJECTION OF CLAIMS 22 AND 23 UNDER 35 U.S.C. §103(a)**

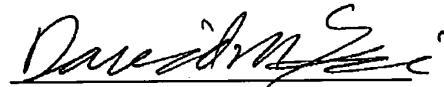
The Examiner rejected claims 22 and 23 under 35 USC §103(a) in view of Nakayama and Gilliland. Applicant respectfully traverses this rejection.

Claims 22 and 23 depend respectively from independent Claim 19 and include all the limitations thereof. Applicant has explained above where Nakayama fails to teach all the

elements of Claim 19. Gilliland teaches a media interface adapter module and fails to provide the teachings missing in Nakayama to support a *prima facie* case of obviousness with respect to Claims 22 and 23. Therefore, Applicant submits that Claims 22 and 23 are nonobvious in view of Nakayama and Gilliland.

In view of the foregoing, Applicant submits that the application is in condition for immediate allowance. In the event any questions or issues remain that can be resolved with a phone call, the Examiner is respectfully requested to initiate a telephone conference with the undersigned.

Respectfully submitted,



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